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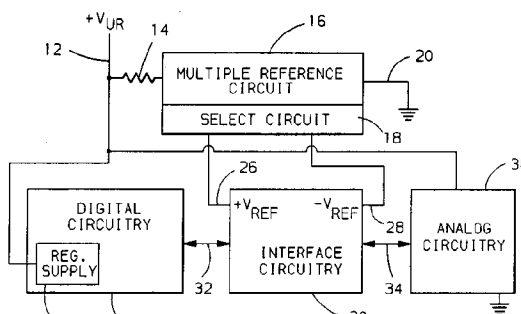
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(54) **Interfacing between analog and digital circuits.**

(57) A circuit comprises interface circuitry (30) between analogue and digital circuitry (22,36). A multiple reference circuit (16) provides a variety of reference voltage signals. The multiple reference circuit (16) is coupled to a selection circuit (18) which selectively couples one of the reference voltage signals to a first reference input (26) of the interface circuitry (30) and selectively couples another of the reference voltage signals to a second reference input (28) of the interface circuitry (30), whereby the first and second reference inputs may be selectively coupled to the reference voltages and the circuit maintains a ratiometric relationship between the digital and analogue circuitry (22,36).



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The subject matter of this application is related to United States patent application Nos 07/944,158, 07/944,154, 07/944,140 and 07/943,964, the disclosures of which are incorporated herein by reference.

This invention relates to a circuit which includes interfacing means for interfacing digital and analogue circuitry.

In certain types of signal processing systems, such as parameter measurement and display systems found in motor vehicles, the system supply voltage is not regulated. When the supply voltage is not regulated, the parameter senders and sensors may provide output signals which vary with the supply voltage. Electronic processing circuitry within the system for processing the sender signals may have built-in regulated voltage supplies, as is required in many integrated circuit systems.

When a sender output signal varies with vehicle supply voltage and the signal processing circuitry includes a regulated supply voltage, the output of the system may indicate that the parameter being measured is varying when in fact it is the vehicle supply voltage which is varying. To add regulated voltage supplies for all of the vehicle senders may be an expensive method of overcoming this problem.

The present invention seeks to provide an improved circuit.

According to another aspect of the present invention, there is provided a circuit as specified in claim 1.

In an embodiment, there can be provided a circuit for parameter measurement and signal processing in systems where the supply voltage may vary and the signal processing circuitry has regulated voltage supplies. It is possible for such a circuit to be substantially unaffected by supply voltage variations and to be suitable for installation into different types of systems.

Advantageously, there is provided means for interfacing sender output signals with signal processing circuitry so that the output of the signal processing circuitry is unaffected by variations in the sender output signals caused by system supply voltage variations. Signal processing circuitry may be interfaced with analogue output devices which may be tied to an unregulated voltage supply, while insulating the output device from the affects of signal variations.

Preferably, various types of sender outputs may be interfaced with processing circuitry. The processing circuitry may in turn be interfaced with various types of output devices requiring various slope and offset values in an output signal.

In an embodiment, there is provided multiple reference circuit means coupled to an unregulated voltage supply and providing multiple reference

signals at various signal levels. Means for interfacing digital and analogue circuitry may be provided and may have positive and negative reference inputs. Selecting means may couple the positive reference input of the interfacing means to a first reference signal of the multiple reference circuit means and the negative reference input of the interfacing means to a second reference signal of the multiple reference circuit means.

An embodiment of the present invention is described below, by way of illustration only, with reference to the accompanying drawings, in which:

Figure 1 is a schematic diagram of an embodiment of circuit;

Figure 2 is an embodiment of circuit for use with analogue-to-digital signal conversion;

Figure 3 is an embodiment of circuit for use with digital-to-analogue conversion;

Figure 4 is an example analogue circuit display;

Figure 5 is a graph of digital signal level against analogue voltage level for the circuits of Figures 1 to 3;

Figures 6A and 6B are a circuit diagram of another embodiment of circuit;

Figure 7 is an example analogue signal source circuit;

Figure 8 is an example analogue signal source circuit for use in systems where the supply voltage is measured; and

Figure 9 is an embodiment of circuit for providing a signal indicative of vehicle supply voltage.

Referring to Figure 1, an unregulated system supply voltage V_{ur} is supplied on line 12 to the system shown. A load resistor 14 couples the supply voltage on line 12 to multiple reference circuit 16, which is grounded at line 20. Line 12 is coupled to digital circuitry 22, which typically has its own regulated voltage supply 24 to supply a fixed regulated voltage to digital circuitry 22. Analogue circuitry 36 also receives power from line 12. An interface circuit 30 interfaces between the digital circuitry 22 and analogue circuitry 36 through lines 32 and 34, performing such functions as analogue-to-digital signal conversion and digital-to-analogue signal conversion as needed. The analogue circuitry 36 has no regulated voltage supply and performs functions which are affected by variations in the supply voltage on line 12.

In order to maintain a constant ratiometric relationship between the analogue and digital circuitry, the output of the interface circuit 30 is rendered insensitive to variations in the functions of analogue circuitry 36 due to variations in the supply voltage.

Multiple reference circuit 16 supplies several reference signals, at a variety of voltage levels, to select circuit 18. Each of the reference signals supplied by multiple reference circuit 16 is a fixed percentage of the supply voltage on line 12. Select

circuit 18 couples a first reference signal from multiple reference circuit 16 to line 26, which is connected to the positive reference of interfacing circuit 30. Select circuit 18 couples a second reference signal from multiple reference circuit 16 to line 28, which is connected to the negative reference of interfacing circuit 30.

Since the reference signals supplied by multiple reference circuit 16 are a fixed percentage of the supply voltage, they vary in proportion to variations in the supply voltage. The interface circuit 30 performs analogue-to-digital conversions and digital-to-analogue conversions in relation to the positive and negative reference signals on lines 26 and 28. If the positive and negative reference signals on lines 26 and 28 vary in proportion to the supply voltage, then the functions of interface circuit 30 vary in proportion to supply voltage. Since the functioning of analogue circuitry 36 also varies in proportion to supply voltage, then the system is rendered insensitive to these variations because the interface to the digital circuitry 22 at line 32 remains insensitive to variations in supply voltage.

If, on the other hand, the positive and negative references for interface circuit 30 were coupled to fixed voltage supplies, the interfacing between the digital and analogue circuitry would vary with variations in supply voltage.

Advantageously, multiple reference circuit 16 provides several reference signals, any two of which may be selected by select circuit 18 as the positive and negative references coupled to lines 26 and 28 and to interface circuit 30. In this manner, a single circuit may be designed for a variety of implementations in which the positive and negative references for interface circuit 30 and the span between those references may vary from implementation to implementation.

Referring to Figure 2, an implementation for use in motor vehicle systems is shown. Analogue circuitry 36 comprises an analogue signal source 50 coupled between the unregulated vehicle voltage supply Vign on line 12 and ground. The analogue signal source 50 outputs an analogue signal on line 54, such as a signal indicative of a vehicle parameter. The analogue signal on line 54 varies in relation to the supply voltage.

The multiple reference circuit 16 comprises a resistor chain 40 which includes a series of resistors fabricated onto an integrated circuit. The resistor chain may comprise anywhere from just a few resistors to several hundred.

Between each resistor in the resistor chain, a tap 41 is placed and carries a signal proportional to the vehicle supply voltage in relation to the total resistance in the resistor chain between the specific tap and ground and the total resistance in the resistor chain between the specific tap and the top

of the chain summed with the resistance of resistor 14. The taps 41 extend along both sides of the resistor chain 40 into the two portions of select circuit 18.

Select circuit 18 comprises two terminals 42 and 44, one terminal running along each side of resistor chain 40 adjacent to the taps 41. One of the terminals is connected to line 26 and the other terminal is connected to line 28. During integrated circuit fabrication, the reference voltages for lines 26 and 28 are set through metal contacts 46 and 48 that are placed in the integrated circuit to couple the desired taps 41 to terminals 42 and 44. Flexibility in the circuit application is easily achieved by varying the contacts 46 and 48 for different circuit applications.

The interface circuit 30 comprises an analogue-to-digital converter 52, which converts the analogue signal on line 54 to a digital signal on bus 56. Lines 26 and 28 are connected to the positive and negative reference inputs of analogue-to-digital converter 52.

The digital output signal of analogue-to-digital converter 52 is a digital signal relational to the magnitude of the signal on line 54 relative to the negative reference signal on line 28 and the positive reference signal on line 26. For example, if the output of analogue-to-digital converter 52 has an eight-bit resolution and the signal on line 54 is below the signal on line 28, the output on bus 56 is zero. If the signal on line 54 is half-way between the negative and positive reference signals on line 28 and 26, the output on bus 56 is 128. Likewise if the signal on line 54 is n% between the negative and positive reference signals on lines 28 and 26, the output on bus 56 is n% of 255.

The signal on line 54 varies with the supply voltage on line 12. For example, assuming that the supply voltage on line 12 is increased temporarily by 5 percent. The signal on line 54, assuming the signal source remains constant, also increases by 5 percent. Additionally, the signals on lines 26 and 28 also increase by 5 percent. It can be shown that because the signals on lines 54, 26 and 28 vary in proportion to the signal on line 12, the signal on bus 56 does not vary. This is true regardless of which taps 41 are selected to be coupled to terminals 42 and 44, as long as the signal on line 26 is greater than the signal on line 28.

Since the signal on bus 56 is not affected by variations in supply voltage on line 12, the digital circuitry 22, which processes the data, is also not affected by the variations in supply voltage on line 12. Digital circuitry 22 may be any sort of suitable processing circuitry, including digital filters, microprocessors and so on, of a type well known to those skilled in the art. Specific examples of digital circuitry 22 are set forth in US patent application

Nos. 944,158, 944,154, 944,140 and 943,964, from which this application claims priority. The disclosures in these applications are incorporated herein by reference. Bus 58 carries the output signal from digital circuitry 22.

Referring to Figure 3, the output of digital circuitry 22 on bus 58 may be used to drive analogue circuitry coupled to the vehicle supply voltage and, like the analogue circuitry 36 in Figure 2, functions in a way which varies in relation to variations in the vehicle supply voltage. In this example also, a ratiometric relationship is maintained between digital circuitry 22 and analogue circuitry 36.

The signal on bus 58 output from digital circuitry 22 is input to digital-to-analogue converter 88, which outputs an analogue signal on line 89 used to drive the display 90 of analogue circuitry 36. The display 90 may be, for example, any type of air core gauge well known to those skilled in the art. The display 90 is connected to the vehicle supply voltage through line 12.

Typically, air core gauges comprise at least two coils surrounding a magnetic rotor. One of the coils is typically coupled between the vehicle supply voltage and ground and the other is coupled between the input signal, line 89, and ground. The coils create a composite magnetic vector which varies in relation to the signal on line 89, the magnetic rotor rotating to align itself with the composite magnetic vector, which causes a pointer attached to a spindle to rotate in the display. Normally, if the vehicle supply voltage varies, the direction of the composite magnetic vector is varied causing the pointer to vary its position in response.

Figure 4 shows an example display including three coil air core gauge 180, comprising coils a, b and c. Coil a is coupled between line 89 and ground and coils b and c are biased by resistors 182 and 184, coupled between the vehicle supply voltage line 12 and ground. Since resistors 182 and 184 are coupled between vehicle supply voltage and ground, the voltage across coils b and c of gauge 180 varies in relation to vehicle supply voltage on line 12. Without compensation, variation in the supply voltage has an effect on the position of pointer 190 relative to graphics 188. However, when the gauge 180 is used with the circuit shown in Figure 3, the signal on line 89 varies with variations in the vehicle supply voltage, varying the magnetic flux produced by coil a in a manner to nullify the effects of variations in the voltage across coils b and c so that there is no net position change in pointer 190 due to variations in vehicle supply voltage.

Referring again to Figure 3, multiple reference circuit 16 comprises a resistor chain 40 as in the circuit shown in Figure 2. The select circuit 18

comprises two sets of transmission gates 70 and 72 and two decoder driver circuits 78 and 80. Each set of transmission gates 70 and 72 comprises one transmission gate for every tap in resistor chain 40. Each decoder/driver 78, 80 has one output line for each transmission gate. Each of the transmission gates 70, 72, when activated, couples one of the lines 26, 28 to one of the taps in resistor chain 40. The control inputs for the transmission gates 70, 72 are connected to the output lines 74, 76 of decoder/drivers 78 and 80.

Input buses 82 and 84 for decoder/drivers 78 and 80 carry digital signals. Each digital signal input to decoder driver 82 selects one of the output lines 74 to control one of the transmission gates 70, coupling one tap in resistor chain 40, carrying a first reference signal, to line 26. Likewise, each digital signal input to decoder driver 80 selects one of the output lines 76 to control one of the transmission gates 72, coupling a second tap in resistor chain 40, carrying a second reference signal, to line 28.

In this manner the signals on buses 82 and 84 control the reference signals on lines 26 and 28. The lines 26 and 28 are coupled to the positive and negative reference inputs of digital-to-analogue converter 88, whereby, similar to analogue-to-digital converter 52 in Figure 2, digital-to-analogue converter 88 maintains an interface between digital circuitry 22 and analogue circuitry 36 in a manner unaffected by variations in the vehicle supply voltage. More specifically and as described above, the functions of display 90 vary in direct relation to the ignition voltage. The positive and negative references to digital-to-analogue converter 88 (signals in lines 26 and 28) also vary in direct relation to ignition voltage. Because of the manner of referencing digital-to-analogue converter 88, the signal on line 89 varies in direct relation to ignition voltage, compensating for the effects of ignition voltage on display 90. The net result is that the functioning of the system is unaffected by variations in ignition voltage.

The circuit shown in Figure 3 is very flexible in application. Buses 82 and 84 may be simply hard-wired to carry specific digital signals to select the reference signals for lines 26 and 28. Alternatively, buses 82 and 84 may be coupled to memory 86, in which data may be stored to control decoder/drivers 78 and 80. In this manner, flexibility in the apparatus shown is achieved by simply changing the data stored in memory 86, or, if the memory is not used, rewiring buses 82 and 84.

Referring to Figure 5, the graph shown illustrates an example offset and slope conversion by interface circuit 30. The offset, point 92, is determined by the negative reference signal. The slope of the conversion is determined by the positive

reference signal, for example points 94 or 96. Since the select circuit 18 allows the positive and negative reference signals to be set from a variety of signals, there is flexibility in the design with respect to the offset and/or slope of the conversion functions performed by interface circuit 30.

Referring to Figure 6, an example of circuit is shown in which the multiple reference circuit 16 comprises a series chain of six resistors 40 with tap points a-g. Taps a, b, c, d, and f are coupled to different data inputs of multiplexers 132 and 134. Taps d, e, f and g are coupled to data inputs of multiplexer 136 and taps c, d, f and g are coupled to the data inputs of multiplexer 137. Lines 112 are coupled to the data inputs of data latches 114-130. The data latches 114-130 latch the signals from lines 112 to their Q outputs when a control signal in lines 152 and 152' is received, thereby addressing multiplexers 132, 134, 136 and 137.

Multiplexers 132 and 134 couple two of the taps a, b, c, d or f to the A and B inputs of multiplexer 140, which couples one of the two input signals to its output. The output of multiplexer 140 is connected to amplifier 144, having a unity gain, which supplies the selected reference signal, a, b, c, d or f on line 26.

Multiplexer 136 couples one of the taps d, e, f or g to the B input of multiplexer 142. The A input of multiplexer 142 is coupled to the output of multiplexer 141. Multiplexer 141 has an A input coupled to the output of multiplexer 137, which is selectively coupled to either the c, d, f or g reference signals. The B input of multiplexer 141 is coupled to the output of sample-and-hold circuit 139, which is used to provide a reference signal such as a ground offset voltage provided on line 151. The sample-and-hold circuit 139 is enabled by the output of AND gate 153.

Multiplexer 138 controls the ground reference for resistor chain 40. When the B input of multiplexer 138 is selected, the tap g of resistor chain 40 is tied to ground. When the A input of multiplexer 138 is selected, the tap g is tied to the output line 28 of amplifier 146. If the input to amplifier 146 is coupled to the output of sample-and-hold circuit 139 via multiplexers 141 and 142, then the g tap of resistor chain 40 is coupled to the reference signal on line 151, which may be a ground offset. The output of multiplexer 142 is coupled to amplifier 146, having unity gain, which provides the selected reference signal on line 28. In this manner, the point g in resistor chain 40 and line 28 may both be tied to the same reference signal.

The select circuit 18 shown in Figure 6 is designed for circuit implementations where only certain combinations of reference points a-g are necessary. For example, in a vehicle system where

it is known that processing circuitry is to be coupled to one of five possible sensors, each having a different output signal range, a system of the type shown in Figure 5 is preferred. The eight control wires 112 may either be coupled to a set of switches for selective circuit control, hard wired in fabrication, or coupled to an eight-bit memory.

Referring to Figure 7, a typical analogue signal source circuit 50 of the type used with the circuitry of Figure 2 is shown. A load resistor 160 and a variable impedance sender 162 are connected in series between the vehicle supply voltage and ground. The impedance of sender 162 varies in relation to a parameter to be measured. As the impedance of sender 162 varies, the voltage level at node 161 varies. A resistor divider comprising resistors 164 and 166 provides a signal on line 54 proportional to the signal at node 161 but at a voltage level suitable for processing by the interface circuit 30.

A question may occur as to how ignition voltage itself is measured in a system where the above-mentioned circuits are used to desensitize the circuitry to changes in ignition voltage. Referring to Figure 8, the circuitry shown may be implemented with the above-mentioned circuits to measure supply voltage.

The analogue signal source 50 comprises a zener diode 170 connected in series with resistor 172 between ignition voltage and ground. An example breakdown voltage for zener diode 170 may be eight volts so that the voltage at point 171 is Vign - 8 volts. In this situation, the voltage at point 171 is no longer a fixed percentage of the ignition voltage. Resistors 164 and 166 provide a signal on line 54 proportional to the signal at point 171.

Since the signal on line 54 is proportional to the signal at point 171, the signal on line 54 is not a fixed percentage of the ignition voltage. The references to the interface circuit 30, however, are a fixed percentage of the ignition voltage so that as the ignition voltage changes, the signal on line 54 changes in a non-ratiometric manner with the reference signals to the interface circuit 30, resulting in the output of interface circuit 30 varying with variations in the ignition voltage. This variation at the output of interface circuit 30 may be used to drive a display in a manner to indicate the level of the ignition supply voltage.

Referring to Figure 9, another example of a circuit for providing an output signal of vehicle ignition voltage is shown. In the circuit, line 200 is supplied with a reference voltage provided by the integrated circuitry. A band-gap reference voltage of 1.27 volts is preferred. The band-gap reference voltage is an accurate reference signal which is relatively stable over varying temperature ranges.

The reference signal on line 200 is coupled to the non-inverting input of comparator 202. The output of comparator 202 is fed to successive approximation register 204, which provides a digital output signal on bus 206. The output signal on bus 206 is coupled to the input of digital-to-analogue converter 208, which has an analogue output on line 209 coupled to the inverting input of comparator 202. Comparator 202, successive approximation register 204 and digital-to-analogue converter 208 operate together in a manner to try to equalize the voltage on line 209 to the reference signal on bus 200.

Digital-to-analogue converter 208 has a positive reference connected to line 26 and a negative reference connected to line 28. Lines 26 and 28 provide positive and negative reference signals proportional to the vehicle ignition voltage on line 12 in accordance with the teachings taught herein. The positive reference signal on line 26 is greater than the reference signal on line 200 and the negative reference signal on line 28 is less than the reference signal on line 200. If the resistor 14 provides a voltage drop so that the voltage at the connection of resistor 14 with the multiple reference circuit 16 is approximately 5 volts when the ignition voltage is 18.5 volts, then it is preferable that line 26 be referenced to 75% of the voltage input to the integrated circuit and that line 28 is referenced to 25% of the voltage input to the integrated circuit.

As the vehicle ignition voltage on line 12 varies, the reference signals on lines 26 and 28 also vary, but the reference signal on line 200 remains fixed. As the signals on lines 26 and 28 vary, the successive approximation register must vary the signal on bus 206 to force digital-to-analogue converter 208 to provide a signal on line 209 equal to the reference signal on line 200. The resulting signal on bus 206 is be used as an indication of vehicle ignition voltage.

If the references given are used, and the successive approximation register and digital-to-analogue converter have a resolution of eight bits, for voltages on line 12 varying from 18.5 to 6.6 volts the range of signals on bus 206 varies from 2 to 235, providing relatively high output resolution.

The vehicle ignition voltage may be displayed by either coupling bus 206 to a digital display or by converting the signal on line 206 to an analogue signal and using the resulting analogue signal to drive an analogue display, such as the display shown in Figure 4.

The above-described circuits provide a system in which analogue circuits connected to unregulated voltage supplies may be interfaced with digital circuits connected to regulated voltage supplies, while maintaining a ratiometric relationship between

analogue and digital data.

The disclosures in United States patent application nos. 944,145, 944,158, 944,154, 944,140 and 943,964, from which this application claims priority, and in the abstract accompanying this application are incorporated herein by reference.

Claims

1. A circuit comprising a multiple reference circuit (16), in use coupled to an unregulated voltage supply, for providing multiple reference signals at a variety of supply levels; interfacing means (30) for interfacing digital and analogue circuitry, the interfacing means including positive and negative reference inputs (26,28); and selecting means (18) for coupling the positive reference input of the interfacing means to a first reference signal of the multiple reference circuit and coupling the negative reference input (28) of the interfacing means to a second reference signal of the multiple reference circuit.
2. A circuit according to claim 1, wherein for analogue circuitry which provides an analogue signal which varies with variations in the unregulated voltage supply; the interfacing means comprises an analogue-to-digital converter (52) for converting on the basis of the positive and negative reference inputs the analogue signal to a digital signal substantially unaffected by variations in the unregulated voltage supply.
3. A circuit according to claim 2, wherein the circuit is adapted to receive an analogue signal indicative of fuel level in a motor vehicle.
4. A circuit according to claim 1, wherein the interfacing means is adapted to convert a digital signal from digital circuitry to an analogue signal for analogue circuitry and includes input means for receiving a digital signal from digital circuitry and output means for outputting a signal to analogue circuitry.
5. A circuit according to claim 4, wherein the circuit is adapted to feed an analogue signal to a display device.
6. A circuit according to any preceding claim, wherein the multiple reference circuit comprises a series of resistors (40) in a resistor chain coupled between the unregulated voltage supply and ground.

7. A circuit according to claim 6, wherein the resistor chain includes a set of series connections (41), each adapted to produce a reference signal proportional to the unregulated supply voltage; the selecting means being adapted selectively to couple one of the series connections to the positive reference signal input and another of the series connections to the negative reference signal input, thereby providing first and second reference signals to the interfacing means.
8. A circuit according to claim 6 or 7, wherein two sets of taps (41) are connected to the series of resistors, one set of taps including a tap (41) connected at each series connection in the resistor series on a first side of the resistor chain, the other set of taps including a tap (41) connected at each series connection of the resistor series on a second side of the resistor chain opposite the first side; the selecting means comprising first and second terminals (42,44) coupled to the positive and negative reference inputs of the interfacing means, the first terminal (42) extending along the first side of the resistor chain in proximity to one set of taps and the second terminal (44) extending along the second side of the resistor chain in proximity to the other set of taps, the first terminal being coupled to a first tap in the one set of taps and the second terminal being coupled to a second tap in the other set of taps.
9. A circuit according to claim 6 or 7, wherein the resistor chain includes a set of series connections (41), a series connection being disposed between each adjacent pair of resistors in the chain; the selecting means comprising first and second pluralities of transmission gates (70,72), the first plurality of gates (70) being coupled to the positive reference input of the interfacing means with each gate thereof coupled to a different series connection in the resistor chain, the second plurality of gates (72) being coupled to the negative reference input of the interfacing means with each gate thereof coupled to a different series connection in the resistor chain, a first decoder/driver (78) including a first set of output lines (74) for controlling the first plurality of transmission gates to couple selectively the positive reference input of the interfacing means to series connections in the resistor chain, and a second decoder/driver (80) including a second set of output lines (76) for controlling the second plurality of transmission gates to couple selectively the negative reference input of the interfacing means to series connections in the resistor chain, thereby in use to couple the positive and negative reference inputs to the first and second reference signals.
10. A circuit according to claim 9, wherein the first and second decoder/drivers are adapted selectively to control the transmission gates in response to control signals stored in a memory.
11. A circuit according to any preceding claim, wherein the interfacing means is operable on the basis of a transfer function having a variable slope and offset.
12. A circuit according to claim 6 or 7, wherein the resistor chain includes a set (A-G) of series connections, a series connection being disposed between each adjacent pair of resistors in the chain; the selecting means comprising at least two multiplexers (132-136), one multiplexer being selectively controllable to couple one of the series connections in the resistor chain to the positive reference input of the interfacing means, the other or another multiplexer being selectively controllable to couple another of the series connections in the resistor chain to the negative reference input of the interfacing means, thereby to couple the positive and negative reference inputs to the first and second reference signals.
13. A circuit according to claim 12, wherein the multiplexers are selectively controllable by control signals stored in a memory.

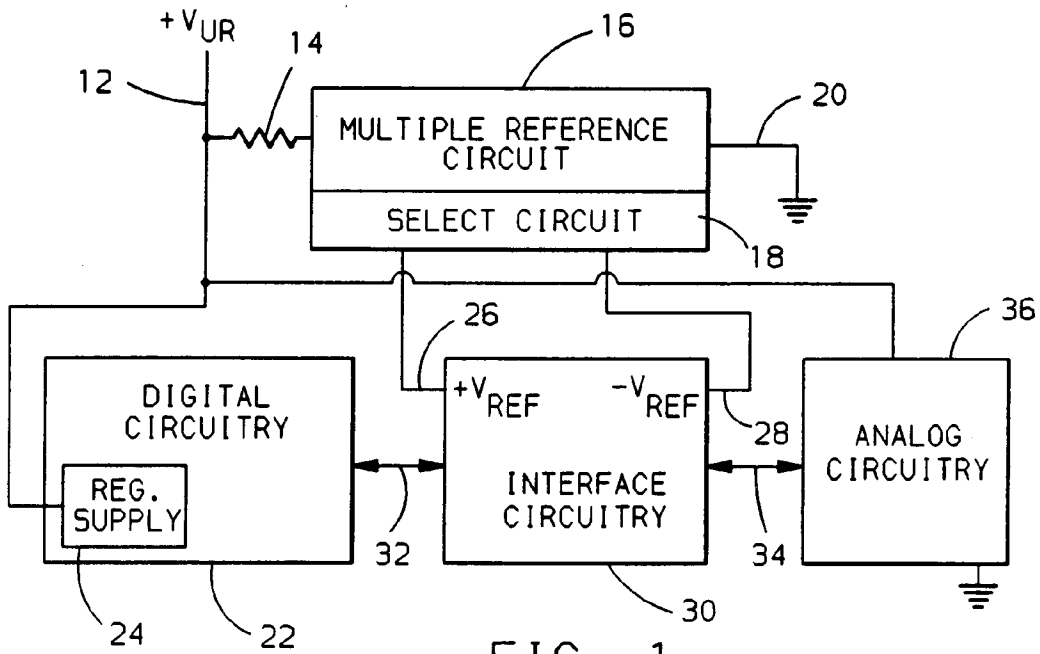


FIG. 1

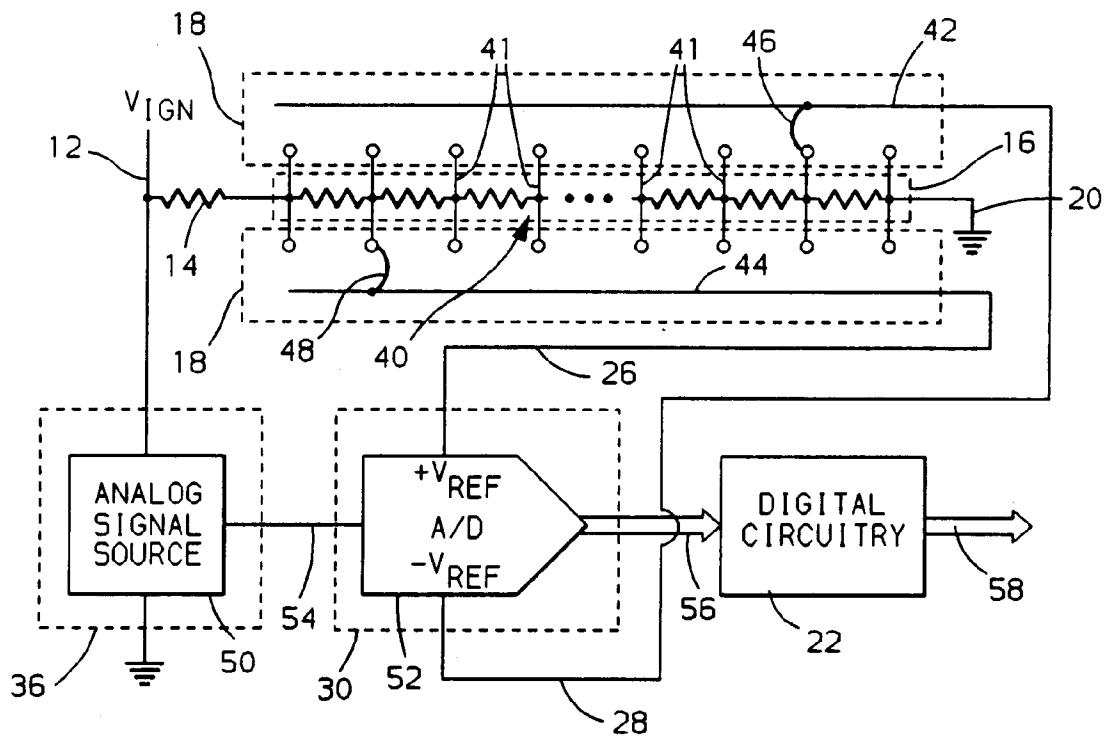


FIG. 2

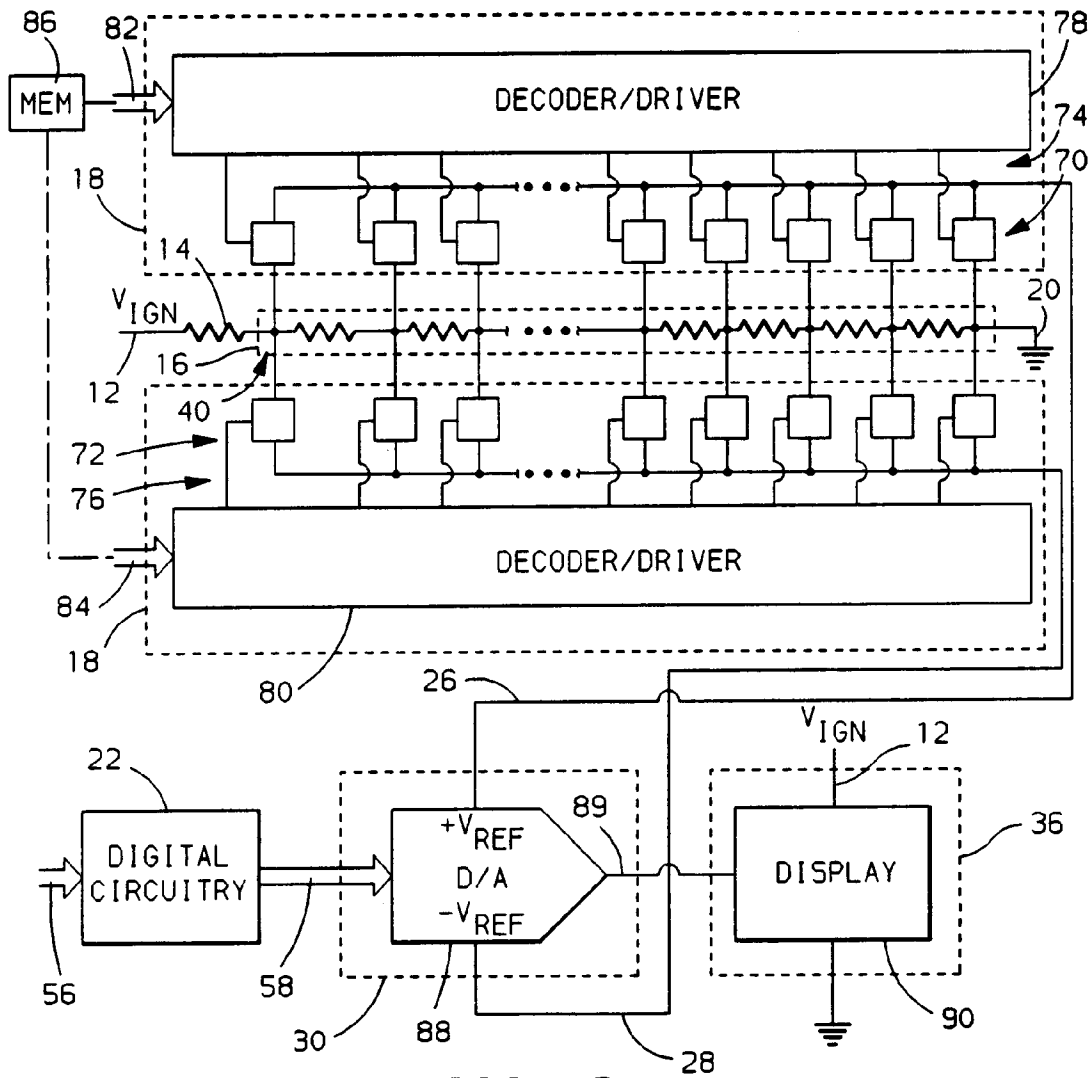


FIG. 3

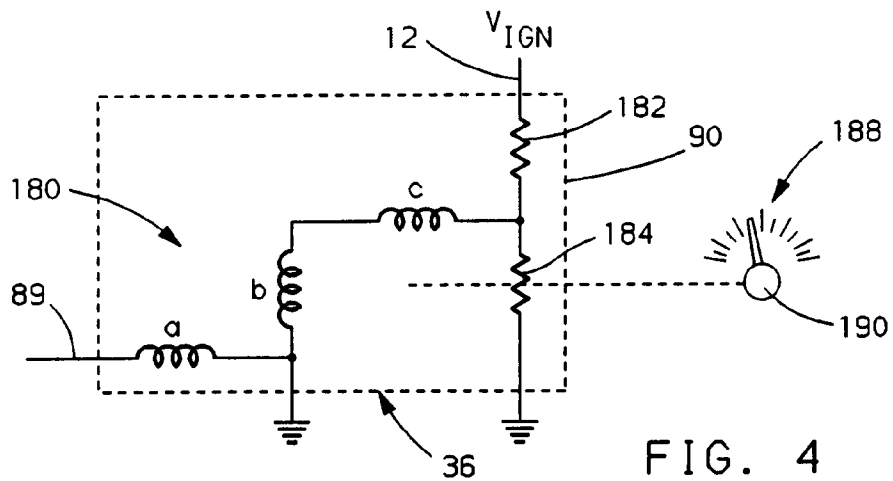


FIG. 4

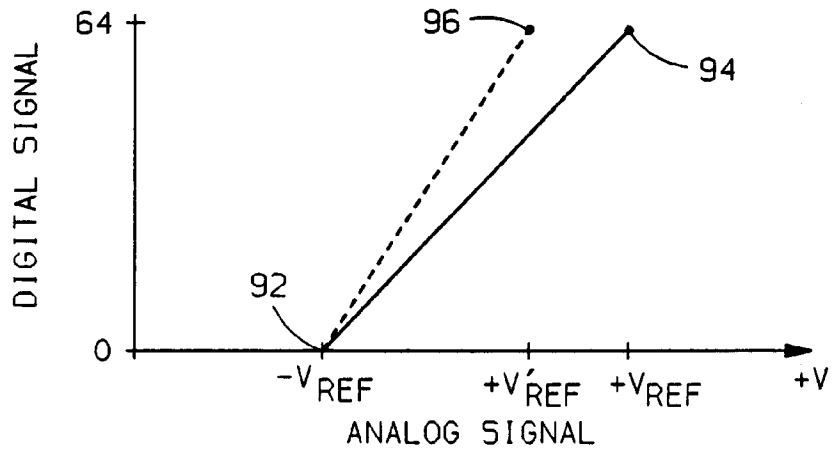


FIG. 5

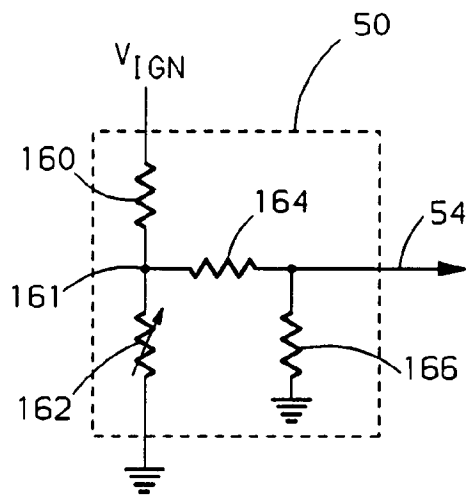


FIG. 7

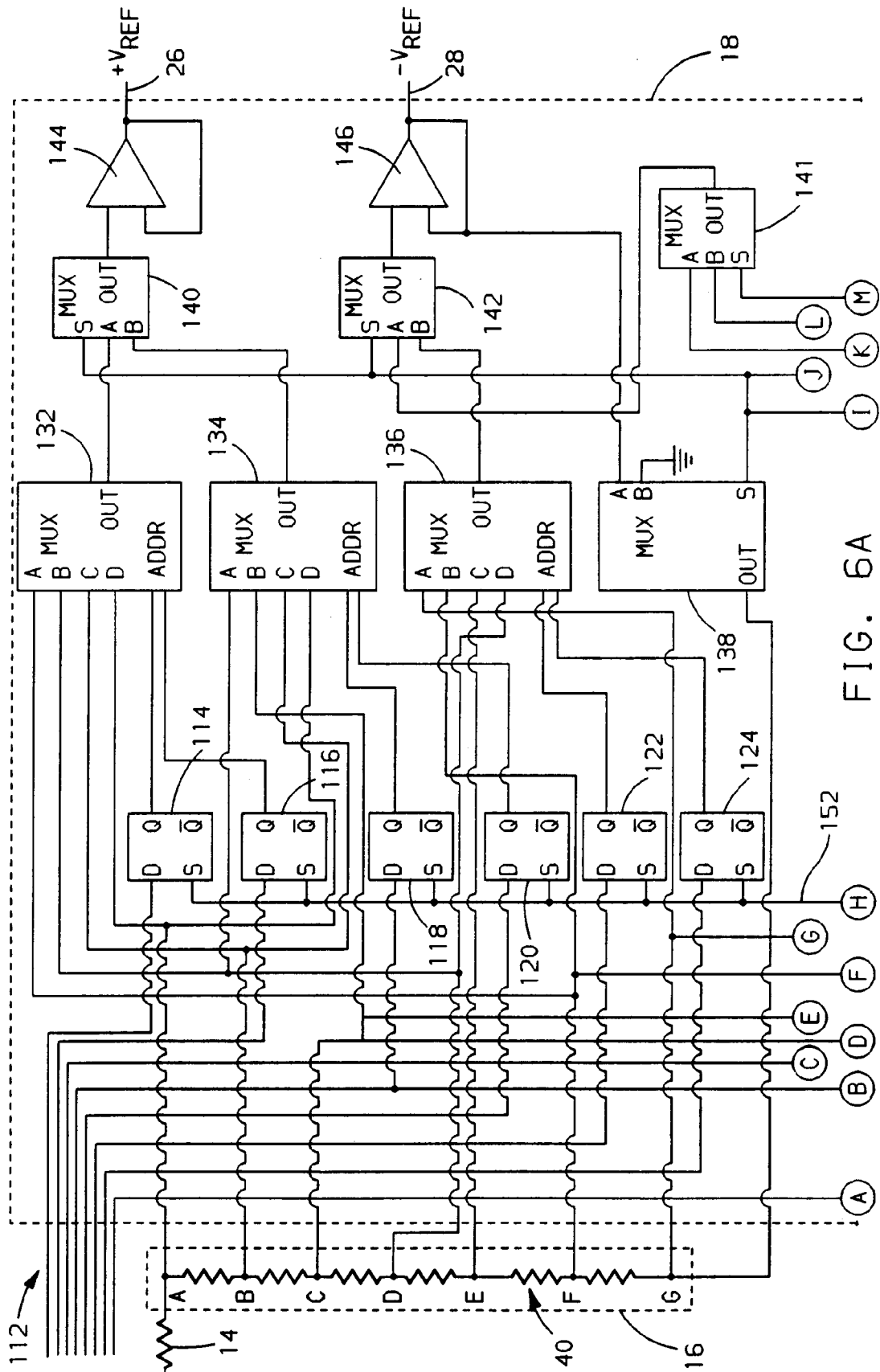


FIG. 6A

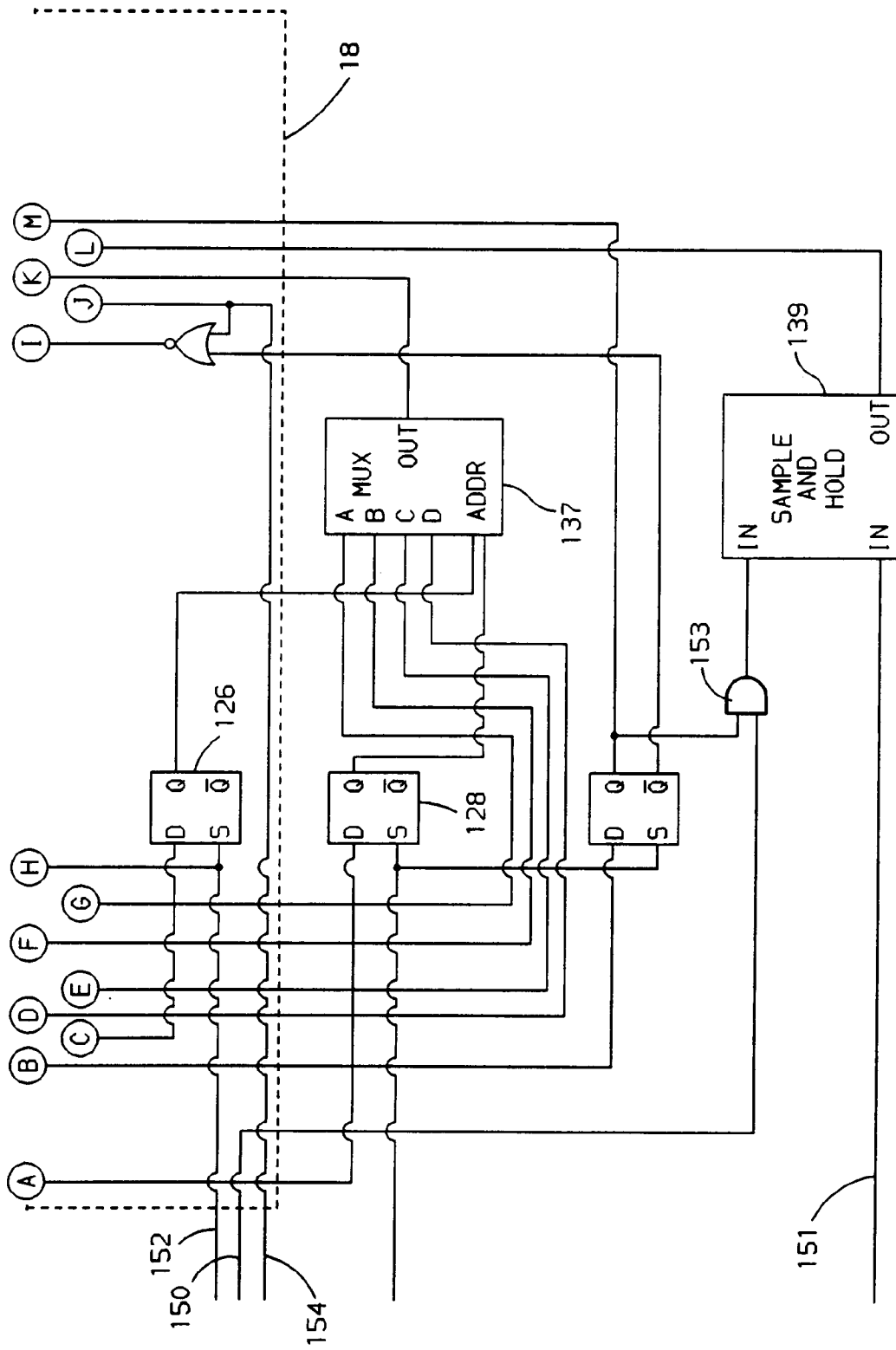


FIG. 6B

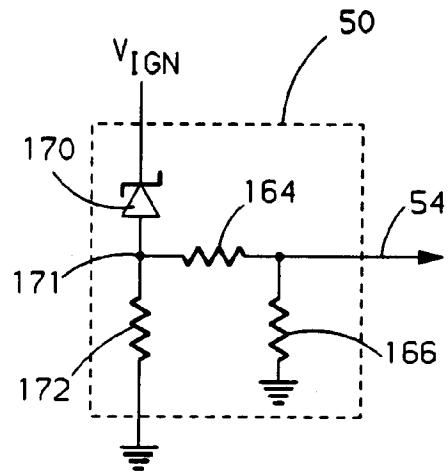


FIG. 8

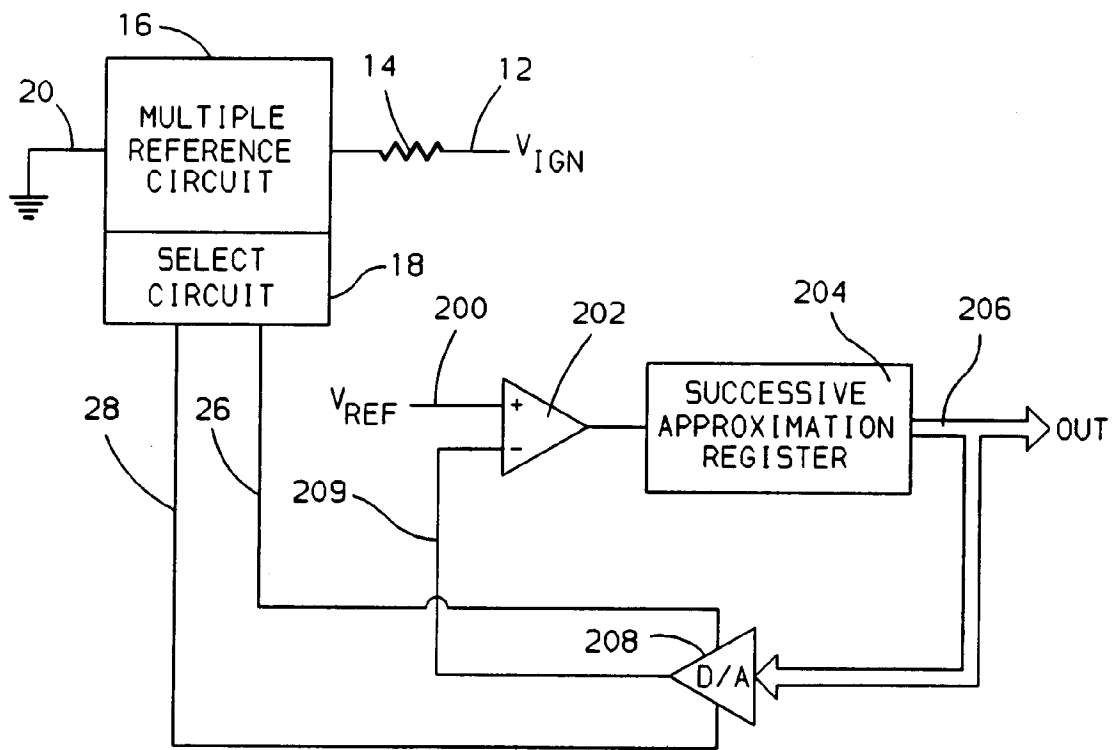


FIG. 9



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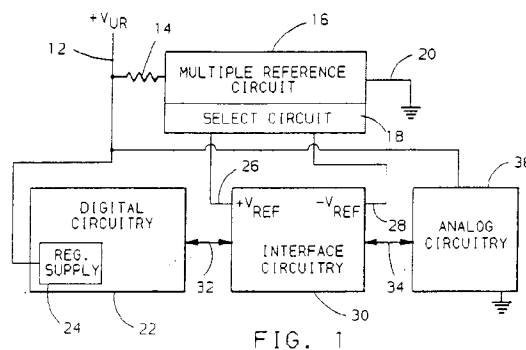
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(54) **Interfacing between analog and digital circuits.**

(57) A circuit comprises interface circuitry (30) between analogue and digital circuitry (22,36). A multiple reference circuit (16) provides a variety of reference voltage signals. The multiple reference circuit (16) is coupled to a selection circuit (18) which selectively couples one of the reference voltage signals to a first reference input (26) of the interface circuitry (30) and selectively couples another of the reference voltage signals to a second reference input (28) of the interface circuitry (30), whereby the first and second reference inputs may be selectively coupled to the reference voltages and the circuit maintains a ratiometric relationship between the digital and analogue circuitry (22,36).





European Patent
Office

EUROPEAN SEARCH REPORT

Application Number
EP 93 20 2275

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.5)
A	FR-A-2 496 360 (SOCIETE POUR L'ETUDE ET LA FABRICATION DES CIRCUITS INTEGRES SPECIAUX) * page 5, line 1; figure 1 * ---	1,2	H03M1/00 G06J1/00 H03M1/06 H03M1/18 G01D3/04
A	US-A-3 886 541 (WATSON ET AL) * column 4, line 35 - line 55; figure 1 * ---	1,2	
A	EP-A-0 130 716 (FUJITSU) * page 1, line 25 - page 10, line 26; figures 1-4 * ---	1,6,7,11	
A	WO-A-81 00653 (LODE) * page 34, line 1 - line 31; figures 1-3 * ---	1,4, 6-10,13	
A	EP-A-0 014 395 (INTERNATIONAL BUSINESS MACHINES) * the whole document * ---	1,2,5,11	
A	EP-A-0 152 930 (ANALOG DEVICES) * claims 1-13; figures 1-2,4 * -----	1,4,6-9	TECHNICAL FIELDS SEARCHED (Int.Cl.5) H03M G01D
The present search report has been drawn up for all claims			
Place of search THE HAGUE		Date of completion of the search 5 October 1994	Examiner Guivol, Y
CATEGORY OF CITED DOCUMENTS X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons & : member of the same patent family, corresponding document			